AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A voltage-to-current converter circuit comprising:

a first metal oxide semiconductor field effect transistor (MOSFET) stage operable in a low to medium input voltage range;

a second MOSFET stage operable in a medium to high input voltage range;

an additive circuit to add current contributions of both the first MOSFET stage and the second MOSFET stage; and

a subtractive circuit for causing ~~to subtract~~ said second MOSFET stage contribution to be subtracted from said first MOSFET stage contribution when both said first MOSFET stage and said second MOSFET stage are operating in a portion of the medium voltage range.

2. (Previously Amended) The circuit of Claim 1 wherein said first MOSFET stage comprises:

a voltage input node at a first MOSFET;

a first current source coupled with the drain of said first MOSFET;

a second current source coupled with the source of said first MOSFET;

a second MOSFET coupled with the drain of said first MOSFET;

a resistor coupled with the source of the first MOSFET;

a bias voltage coupled with the gate of said second MOSFET;

a third MOSFET having a gate and drain coupled with a source of said second MOSFET; and

a fourth MOSFET mirrored to said third MOSFET.

3. (Previously Amended) The circuit of Claim 1 wherein said second MOSFET stage comprises:

a voltage input node at a first MOSFET;

a current source coupled with the source of said first MOSFET;

a second MOSFET source coupled with the source of said first MOSFET;

a resistor coupled with the drain of the first MOSFET;

a bias voltage coupled with the gate of said MOSFET;

a third MOSFET having a gate and source coupled with said second MOSFET; and

a fourth MOSFET mirrored to said third MOSFET.

4. (Original) The circuit of Claim 1 wherein said additive circuit generates an output current and operates from the low voltage range to the high voltage range to provide a rail-to-rail linear voltage-to-current output.

5. (Original) The circuit of Claim 1 wherein said additive circuit combines an output current of said first MOSFET stage with the output current of said second

MOSFET stage to achieve a linear current slope for an input voltage range from 0V to a maximum voltage (VPWR).

6. (Original) The circuit of Claim 5 wherein the output current versus input current slopes for both said first MOSFET stage and said second MOSFET stage of the circuit are matched using an equivalent load resistor in both said first MOSFET stage and said second MOSFET stage.

7. (Original) The circuit of Claim 1 wherein said subtractive circuit comprises a first MOSFET with a gate coupled with the gate of a current output MOSFET of the second MOSFET stage and a source coupled with a source of a current output MOSFET of the first MOSFET stage.

8. (Original) The circuit of Claim 7 wherein when both the first MOSFET stage and the second MOSFET stage are operational, the first MOSFET stage removes the output current contributions of the second MOSFET stage using the subtractive circuit leaving the output current of the circuit dependent only on the FIRST second MOSFET stage contribution.

9. (Cancelled)

10. (Currently Amended) A voltage to current converter circuit comprising:

a positive channel metal-oxide semiconductor (PMOS) stage operable in a low to medium voltage range;

a negative channel metal-oxide semiconductor (NMOS) stage operable in a medium to high voltage range;

an additive circuit to add current contributions of both the NMOS stage and the PMOS stage from the low voltage range to the high voltage range to provide a rail-to-rail linear voltage-to-current output; and

a subtractive circuit to subtract said NMOS ~~PMOS~~ stage current contribution when both said NMOS stage and said PMOS stage are operating in the medium voltage range.

11. (Original) The circuit of Claim 10 wherein said PMOS stage comprises:

a voltage input node at a first PMOS transistor;

a first current source coupled with the drain of said first PMOS transistor;

a second current source coupled with the source of said first PMOS transistor;

a resistor coupled with the source of the first PMOS transistor;

an NMOS transistor drain coupled with the drain of said first PMOS transistor;

a bias voltage coupled with the gate of said NMOS transistor;

a second PMOS transistor having a gate and drain coupled with a source of said NMOS transistor; and

a third PMOS transistor mirrored to said second PMOS transistor.

12. (Previously Amended) The circuit of Claim 10 wherein said NMOS stage comprises:

a voltage input node at a first NMOS transistor;

a current source coupled with the source of said first NMOS transistor;

a PMOS transistor source coupled with the source of said first NMOS transistor;

a resistor coupled with the drain of the NMOS transistor;

a bias voltage coupled with the gate of said PMOS transistor;

a second NMOS transistor having a gate and source coupled with said PMOS transistor; and

a third NMOS transistor mirrored to said second NMOS transistor.

13. (Original) The circuit of Claim 10 wherein said additive circuit combines an output current of said PMOS stage with the output current of said NMOS stage to achieve a linear current slope for an input voltage range from 0 Volts to a maximum voltage (VPWR).

14. (Original) The circuit of Claim 13 wherein the output current versus input current slopes for both said PMOS stage and said NMOS stage of the circuit are matched using an equivalent load resistor in both said PMOS stage and said NMOS stage.

15. (Original) The circuit of Claim 10 wherein said subtractive circuit comprises a first NMOS transistor with a gate coupled with the gate of a current output NMOS transistor of the NMOS stage and a source coupled with a source of a current output PMOS transistor of the PMOS stage.

16. (Original) The circuit of Claim 15 wherein when both the PMOS stage and the NMOS stage are operational, the PMOS stage will remove the output current contributions of the NMOS stage using the subtractive circuit leaving the output current of the circuit dependent only on the PMOS stage contribution.

17. (Original) The circuit of Claim 15 wherein when both the PMOS stage and the NMOS stage are operational, the NMOS stage will remove the output current contributions of the PMOS stage using the subtractive circuit leaving the output current of the circuit dependent only on the NMOS stage contribution.

18. (Previously Amended) A voltage-to-current converter circuit comprising:

a first voltage-to-current converter circuit operational from a low to a mid input voltage range;

a second voltage-to-current converter circuit operational from a mid to a high input voltage range; and

a current compensation circuit coupled with said first and second voltage-to-current converter circuits, wherein said current compensation circuit removes the input of said second voltage-to-current converter during the mid voltage range when both said first and said second voltage-to-current converters are operational.

19. (Original) The voltage-to-current converter of Claim 18 further comprising:

a current additive circuit coupled with said first and said second voltage-to-current converter circuits, wherein said current additive circuit outputs the current from both the first and the second voltage-to-current converter circuits as a linear current slope for an input voltage ranging from 0 Volts to a maximum voltage (Vpwr).

20. (Original) The voltage-to-current converter of Claim 18, wherein when both the first and said second voltage-to-current converter circuits are operational, the current compensation circuit will remove the output current contributions of the second voltage-to-current converter circuit leaving the output current of the voltage-to-current converter circuit dependent only on the first voltage-to-current converter circuit contribution.